

FIG. 1A
(PRIOR ART)



Material Transport Method
Harold L. Trammell
09/602,162
M-9210 US

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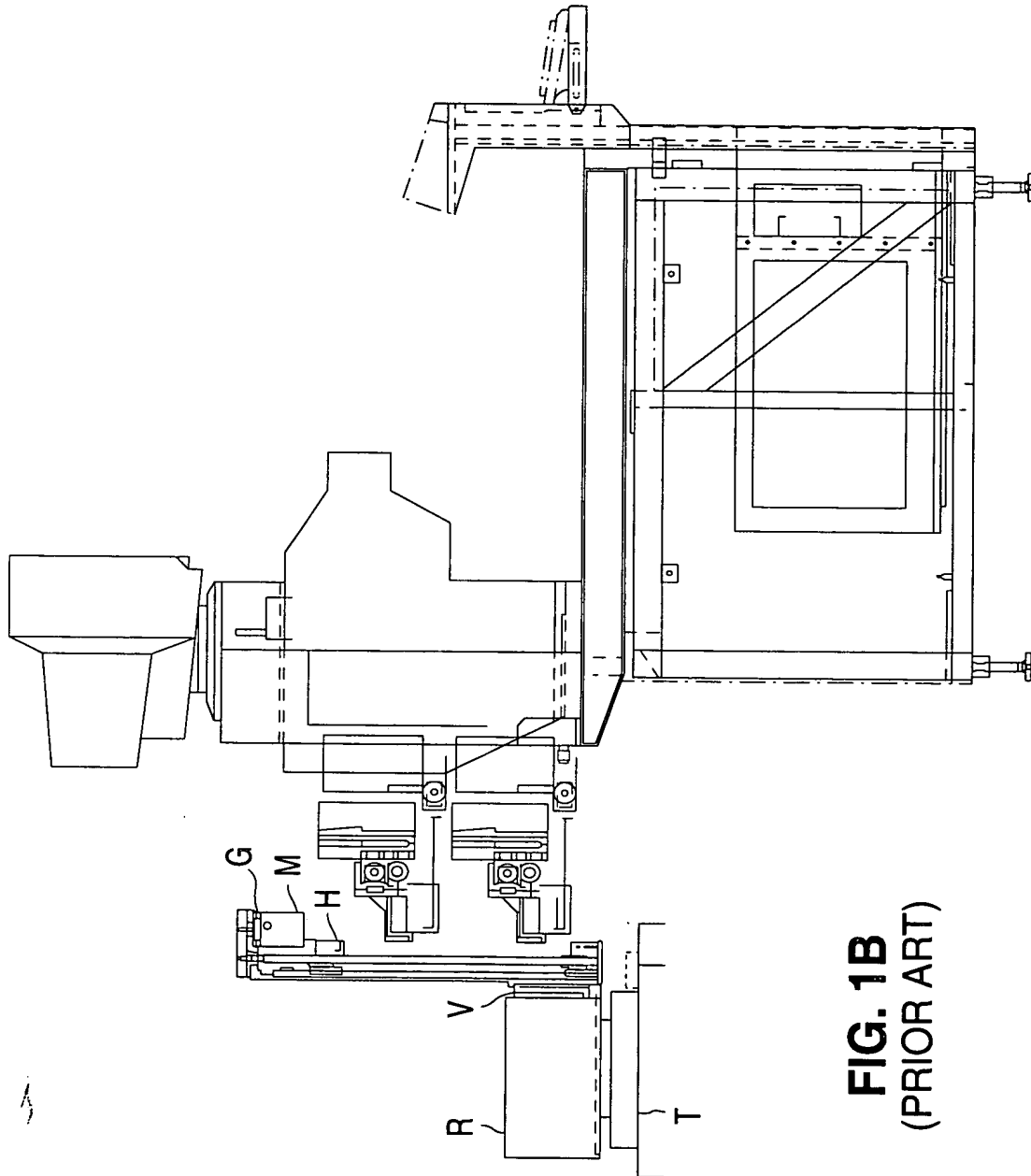
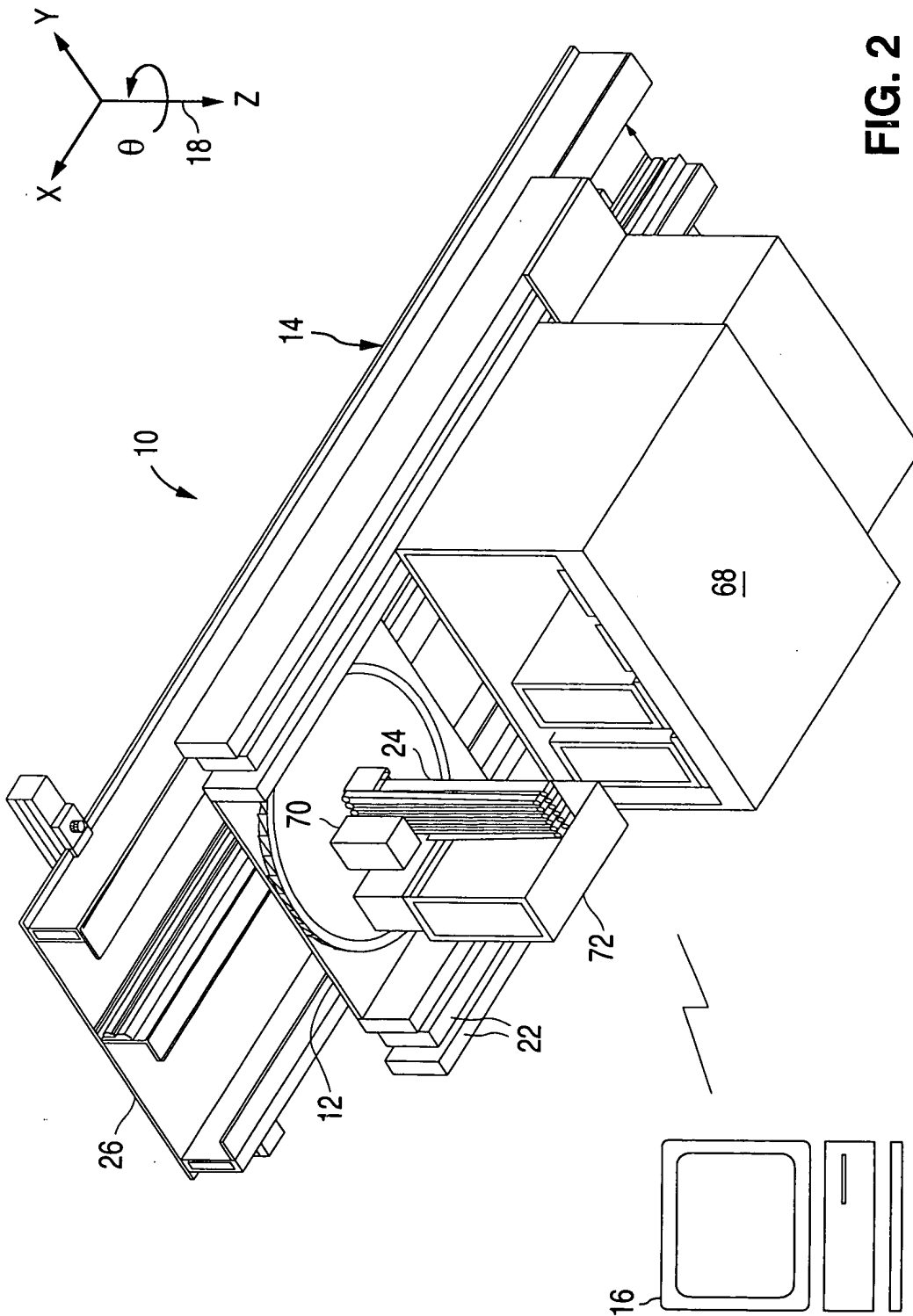


FIG. 1B
(PRIOR ART)



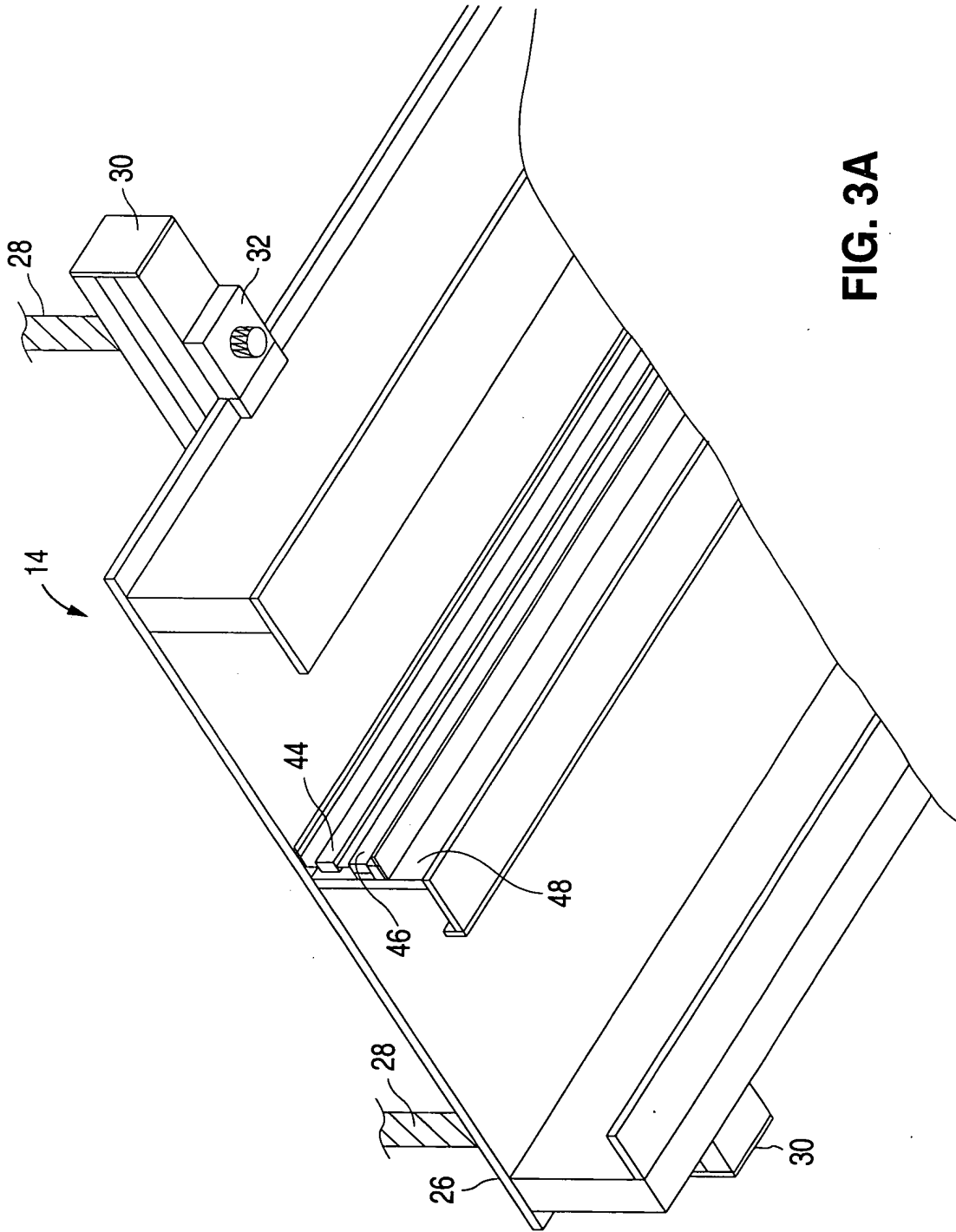
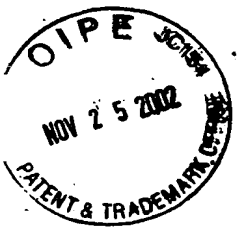


FIG. 3A



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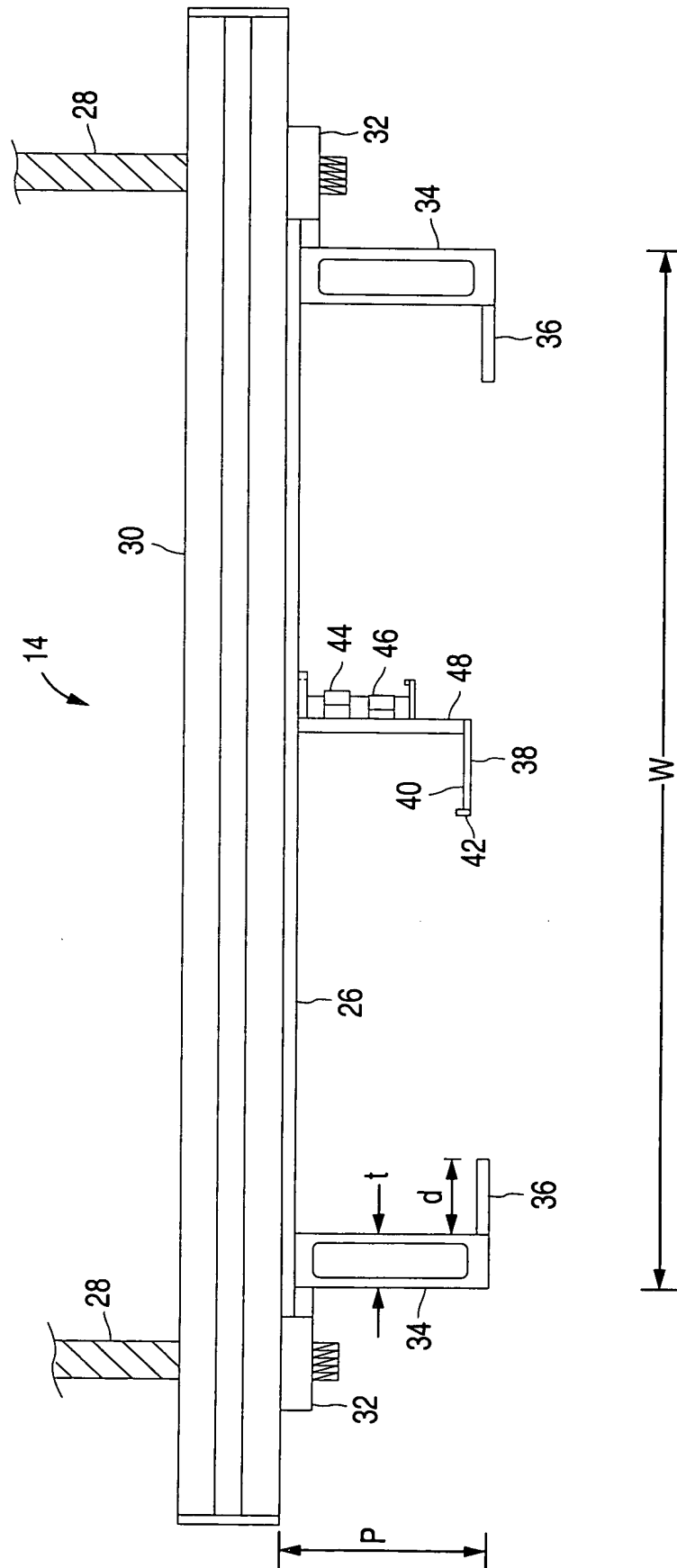
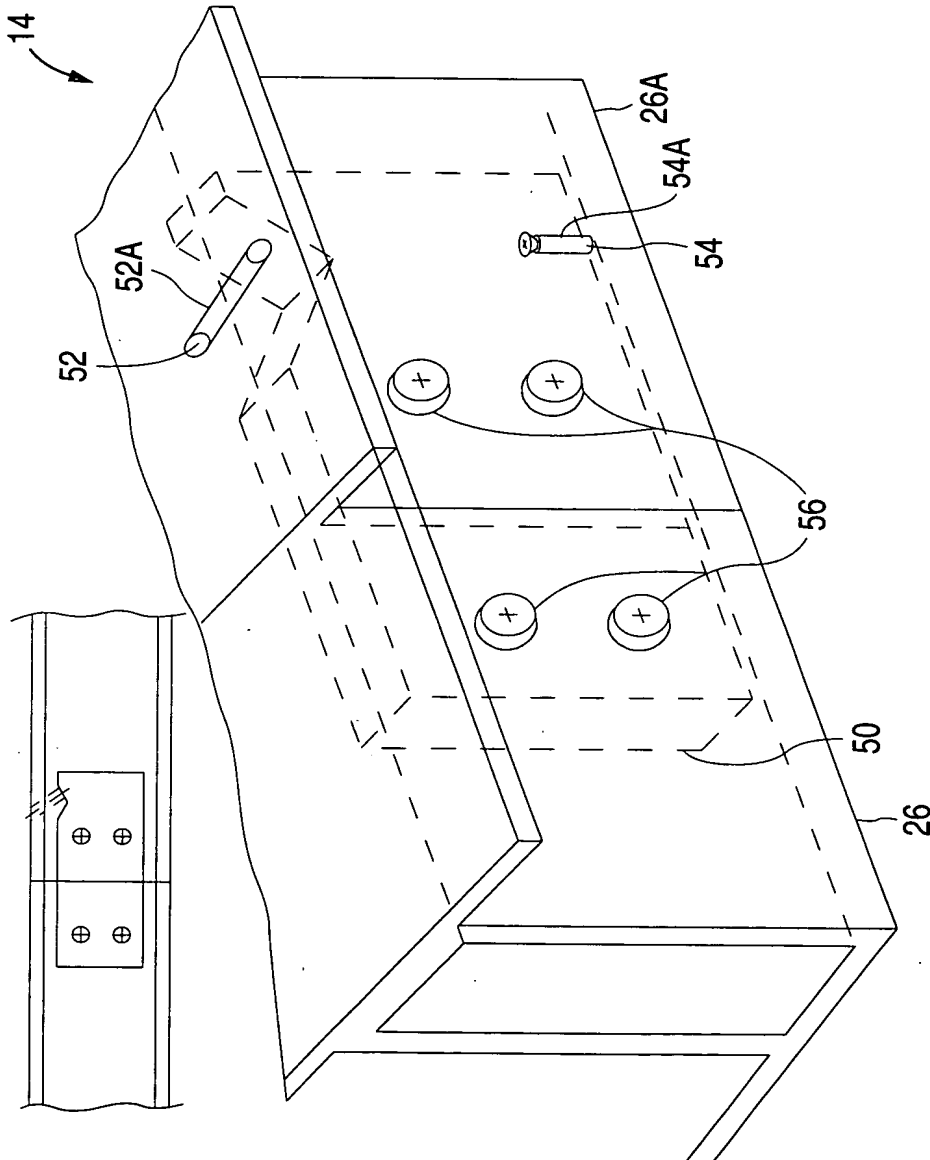


FIG. 3B



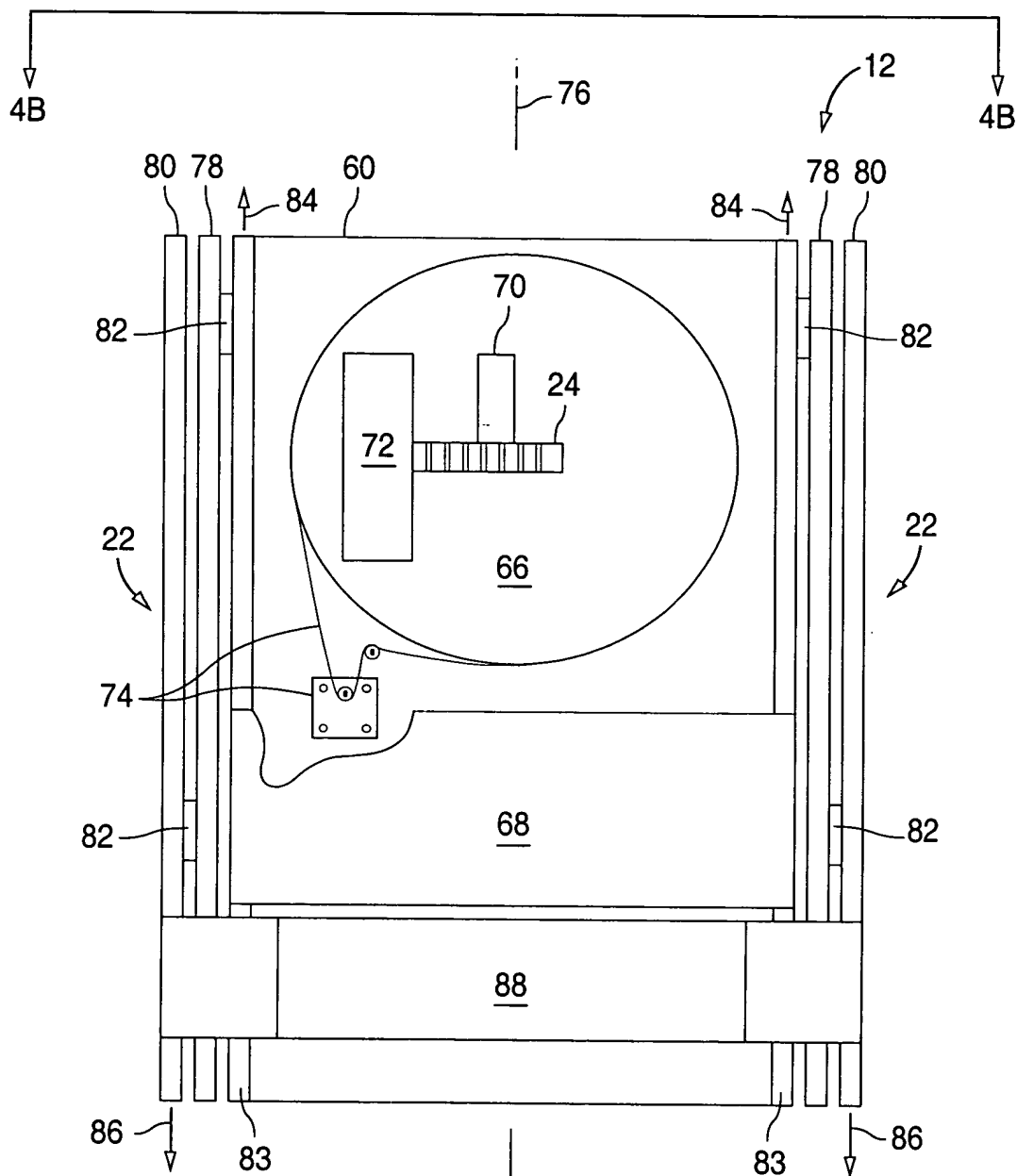
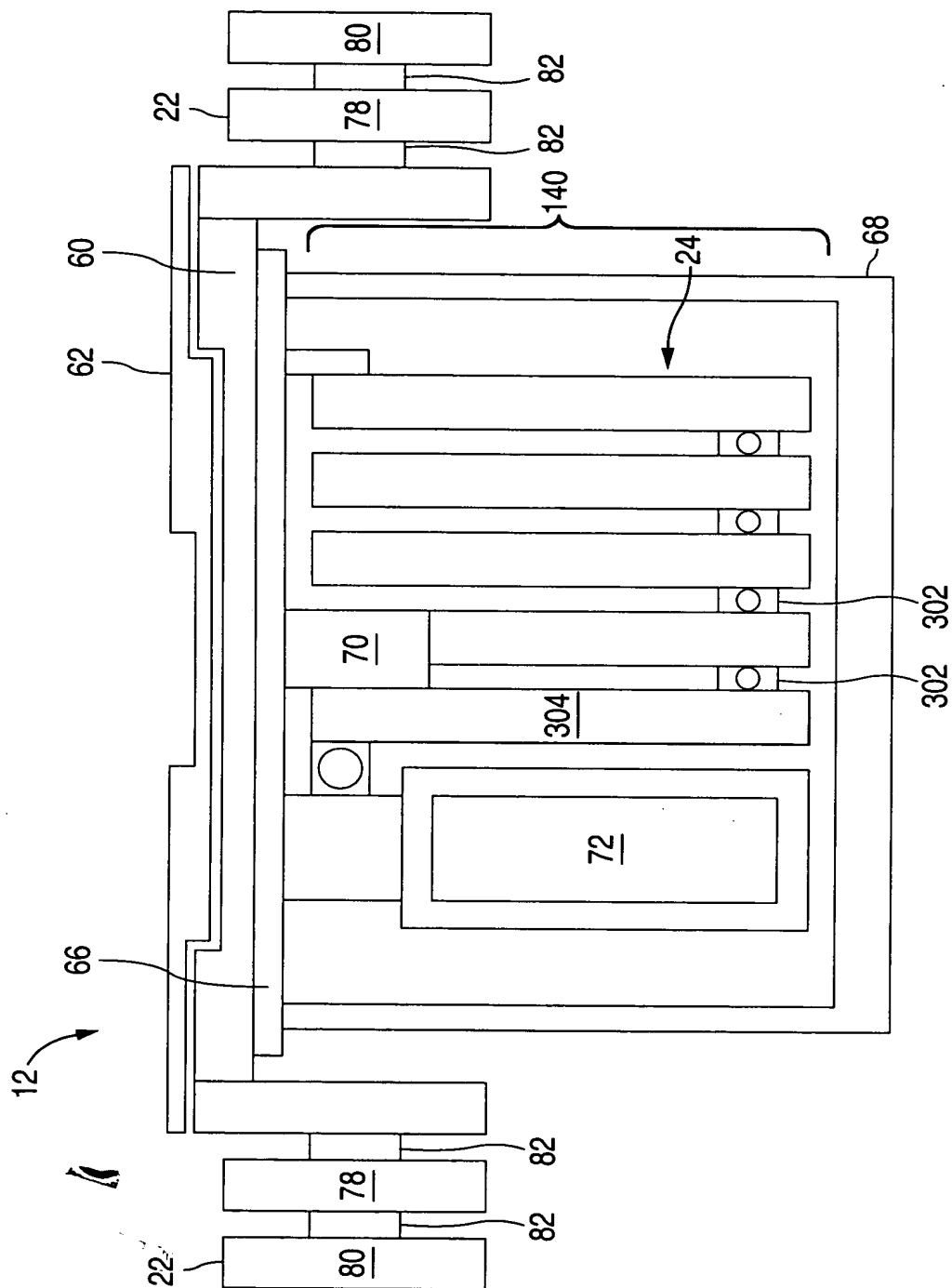


FIG. 4A

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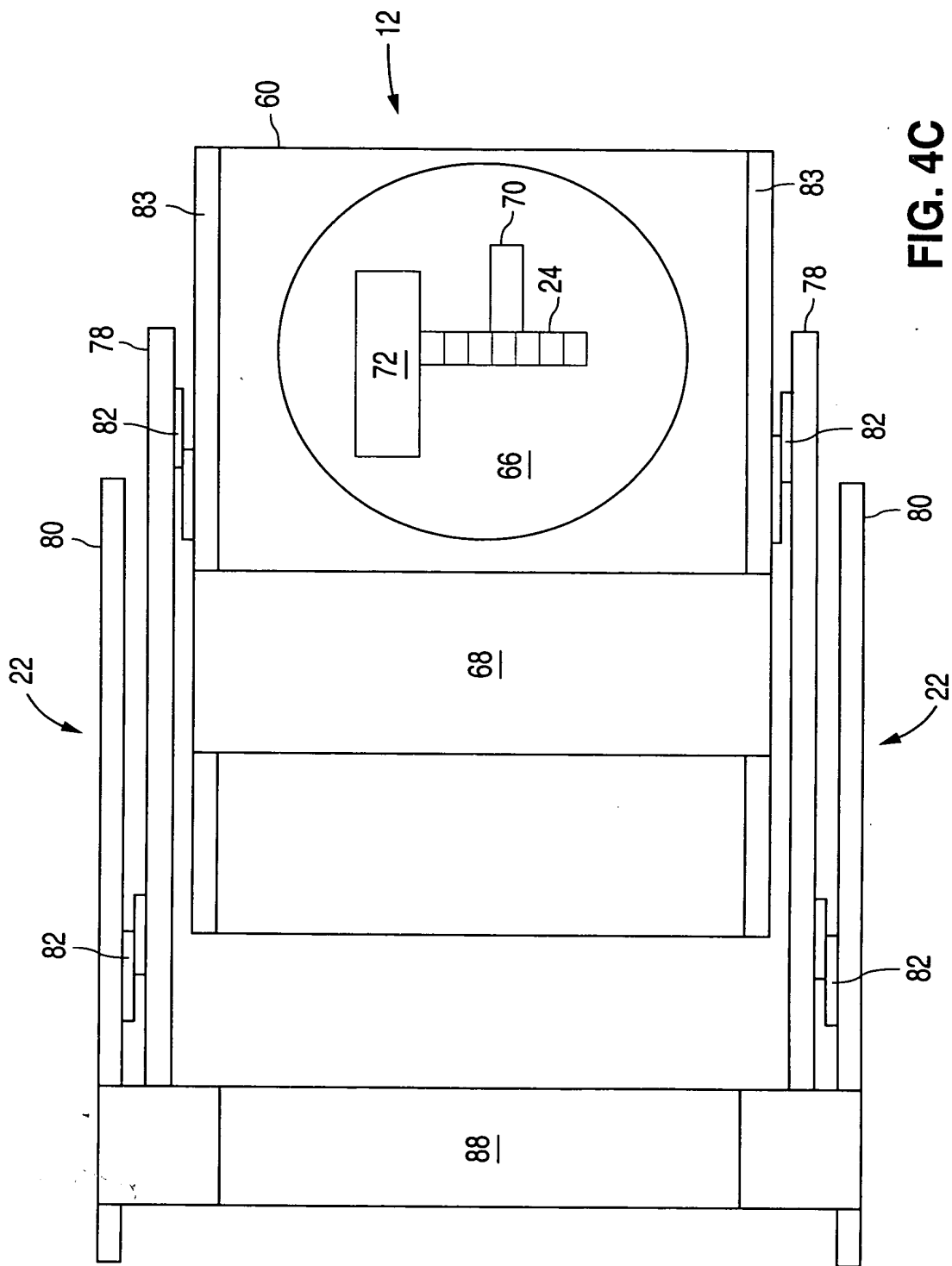


FIG. 4C

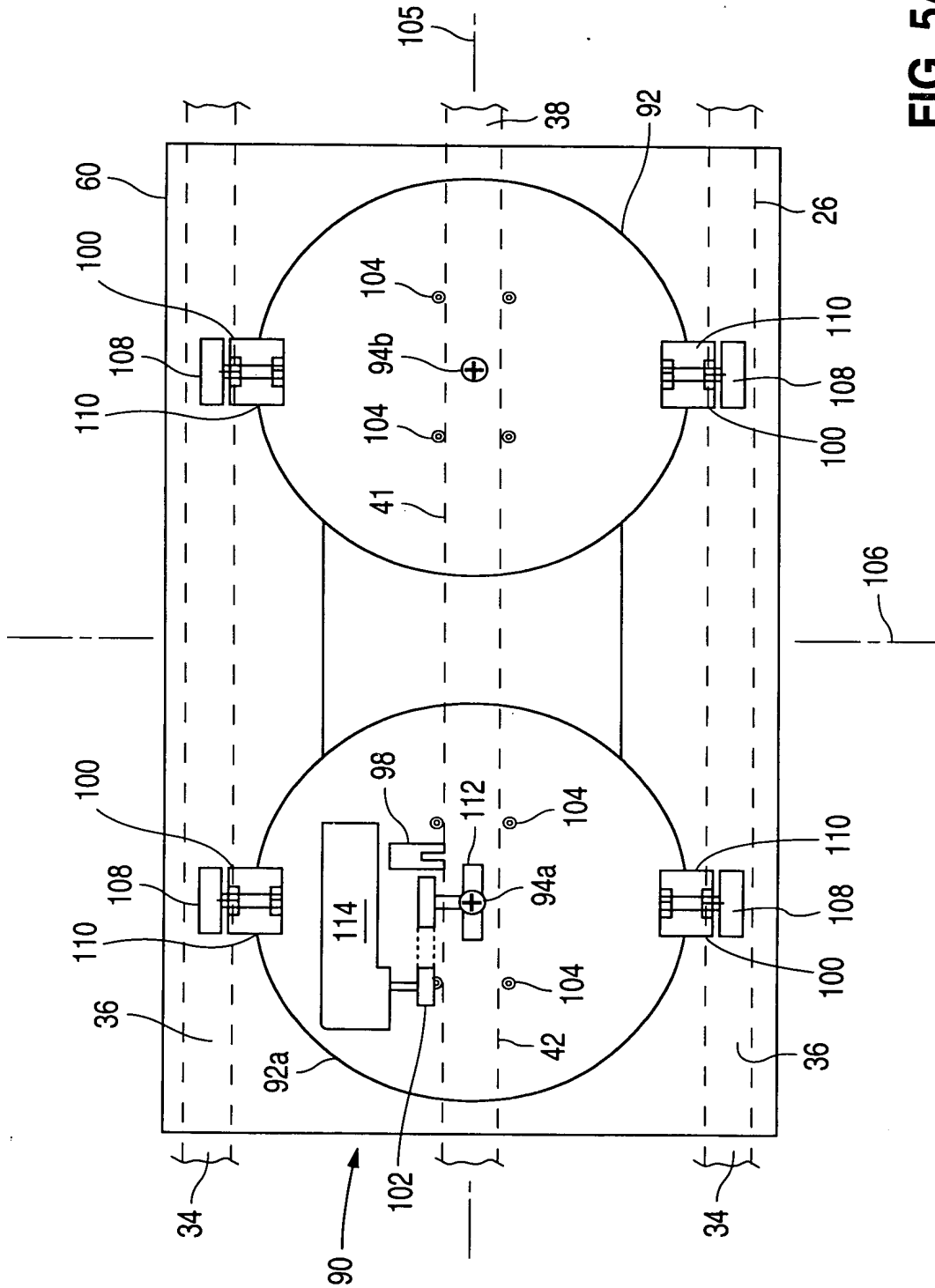


FIG. 5A

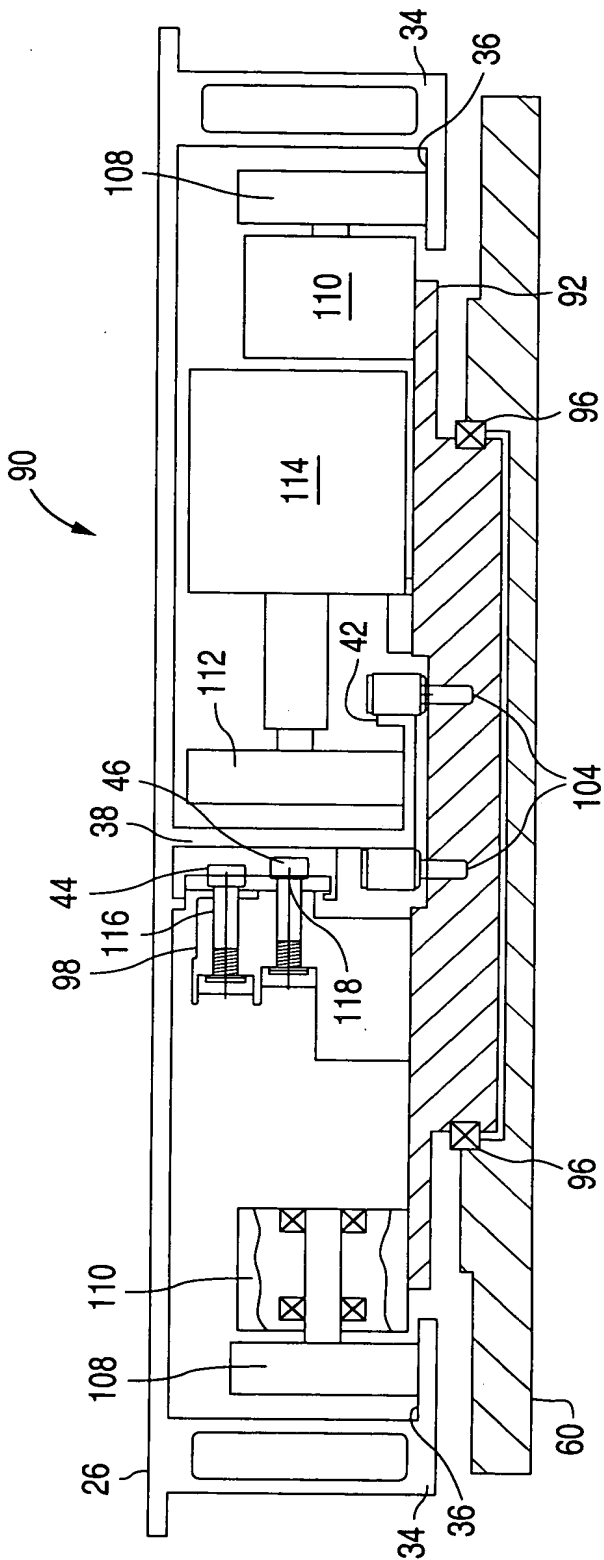


FIG. 5B



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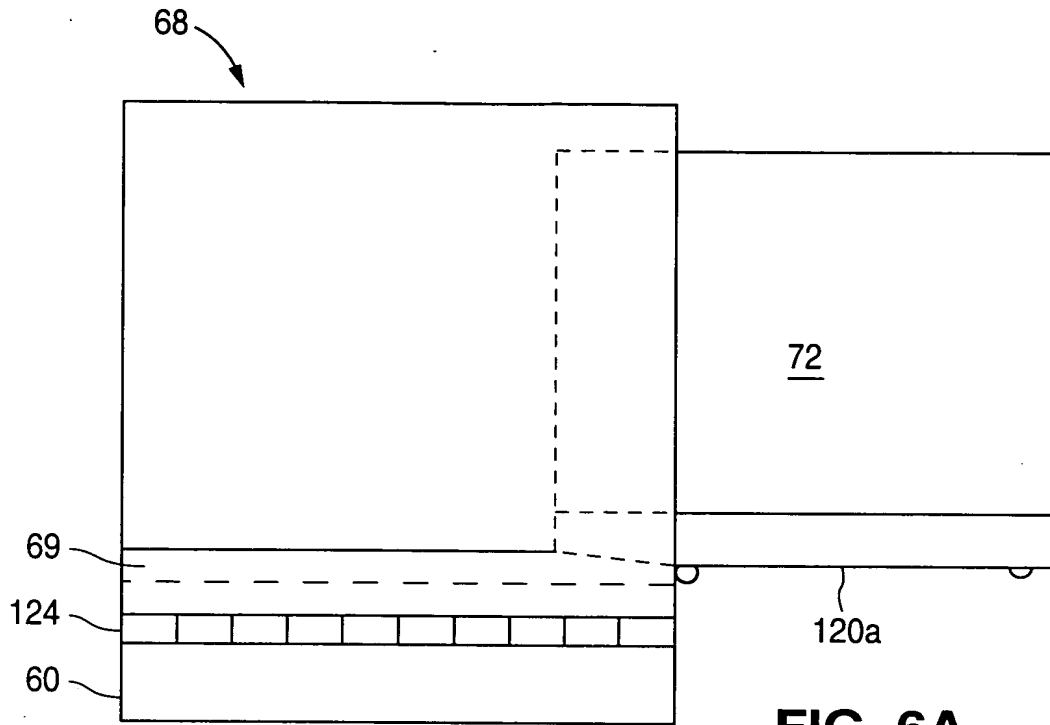


FIG. 6A

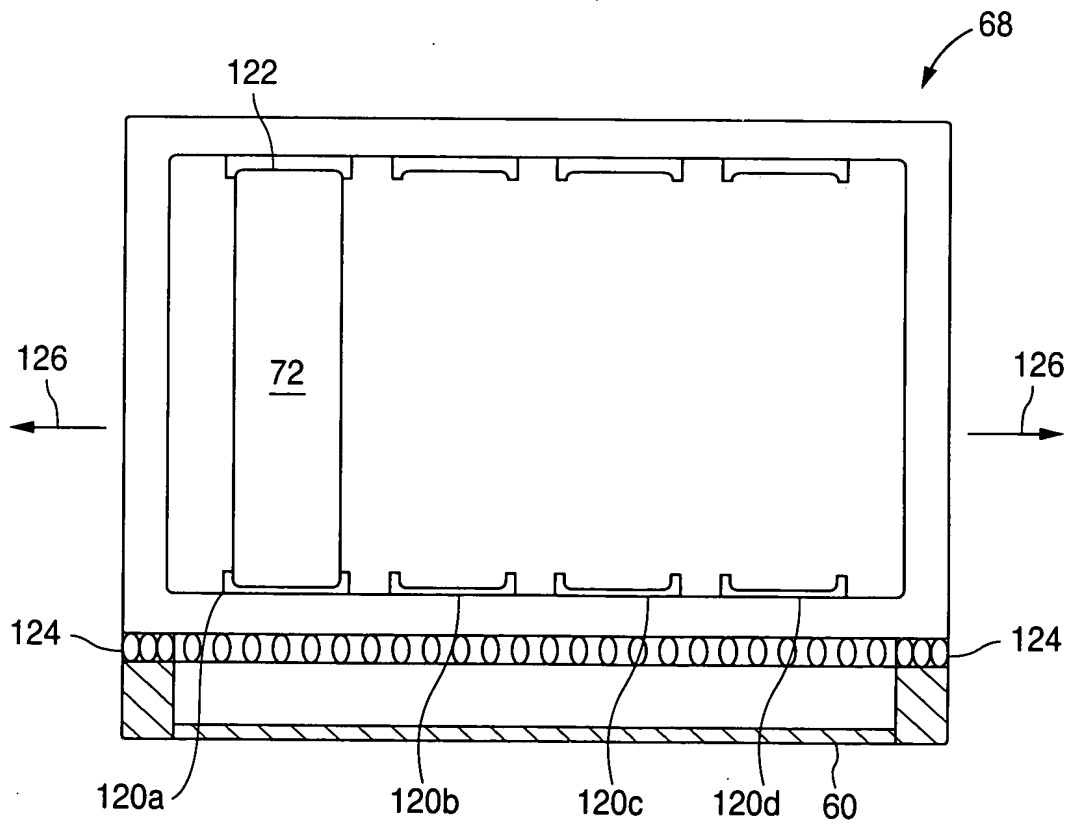


FIG. 6B

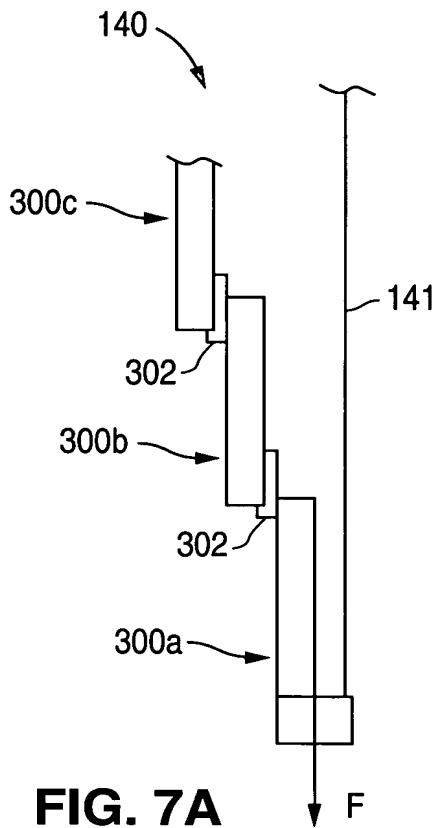


FIG. 7A

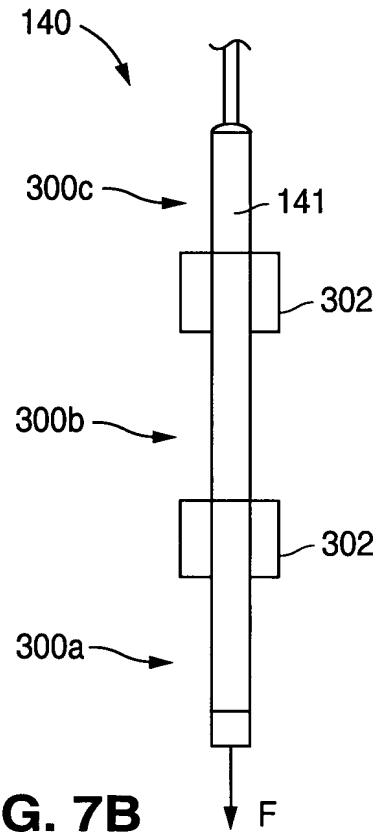


FIG. 7B

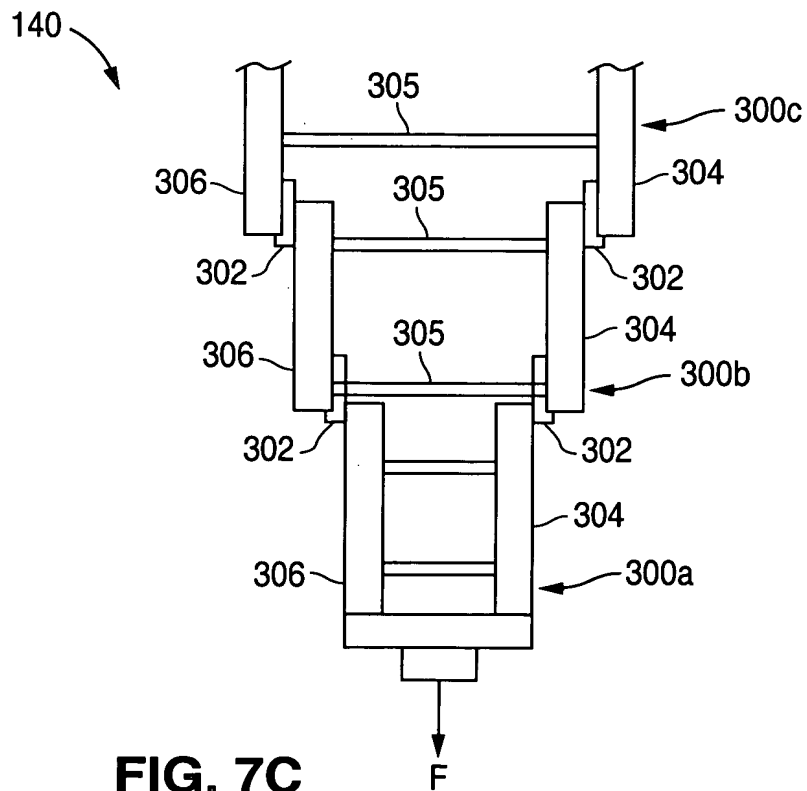


FIG. 7C

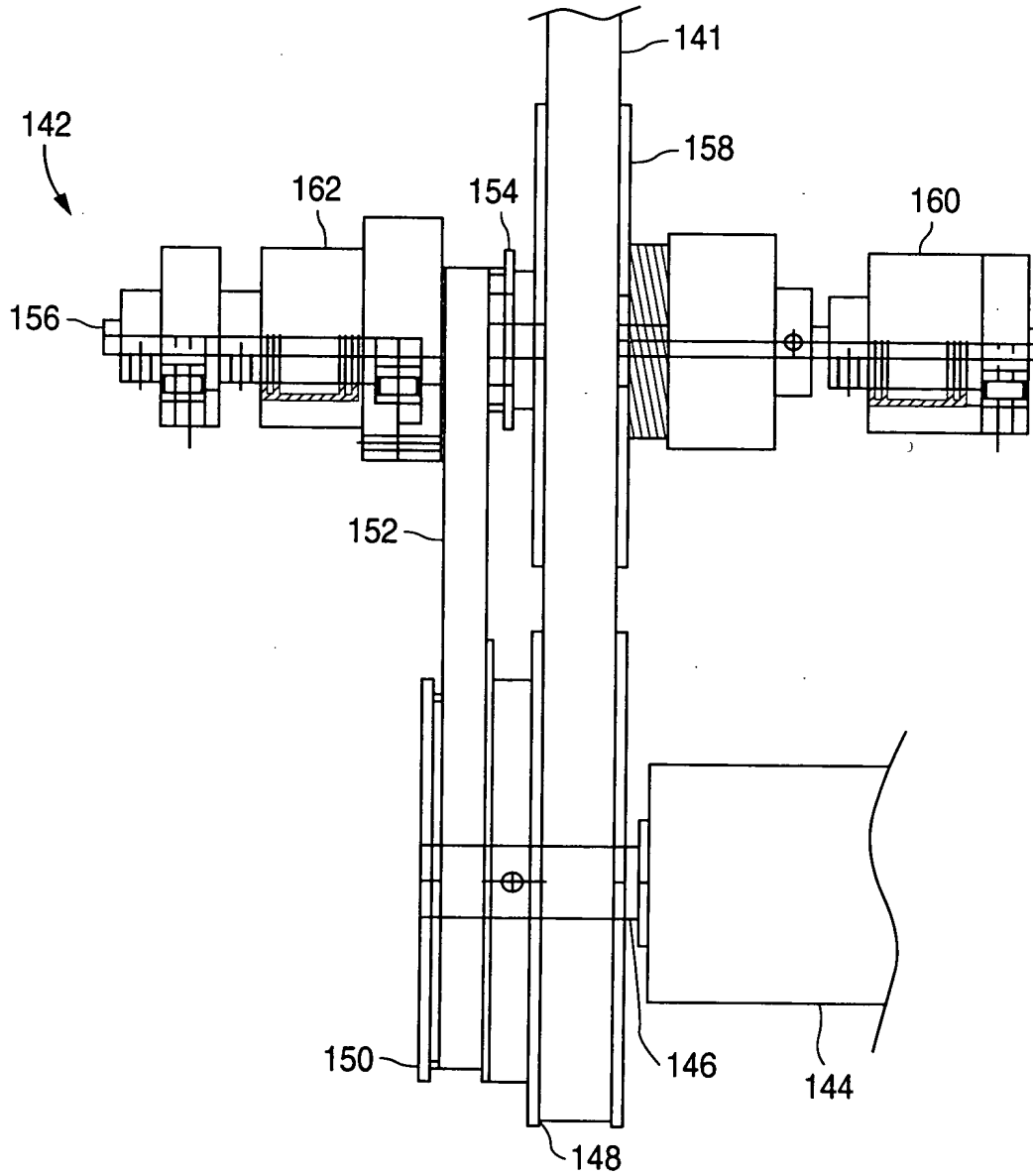


FIG. 8A

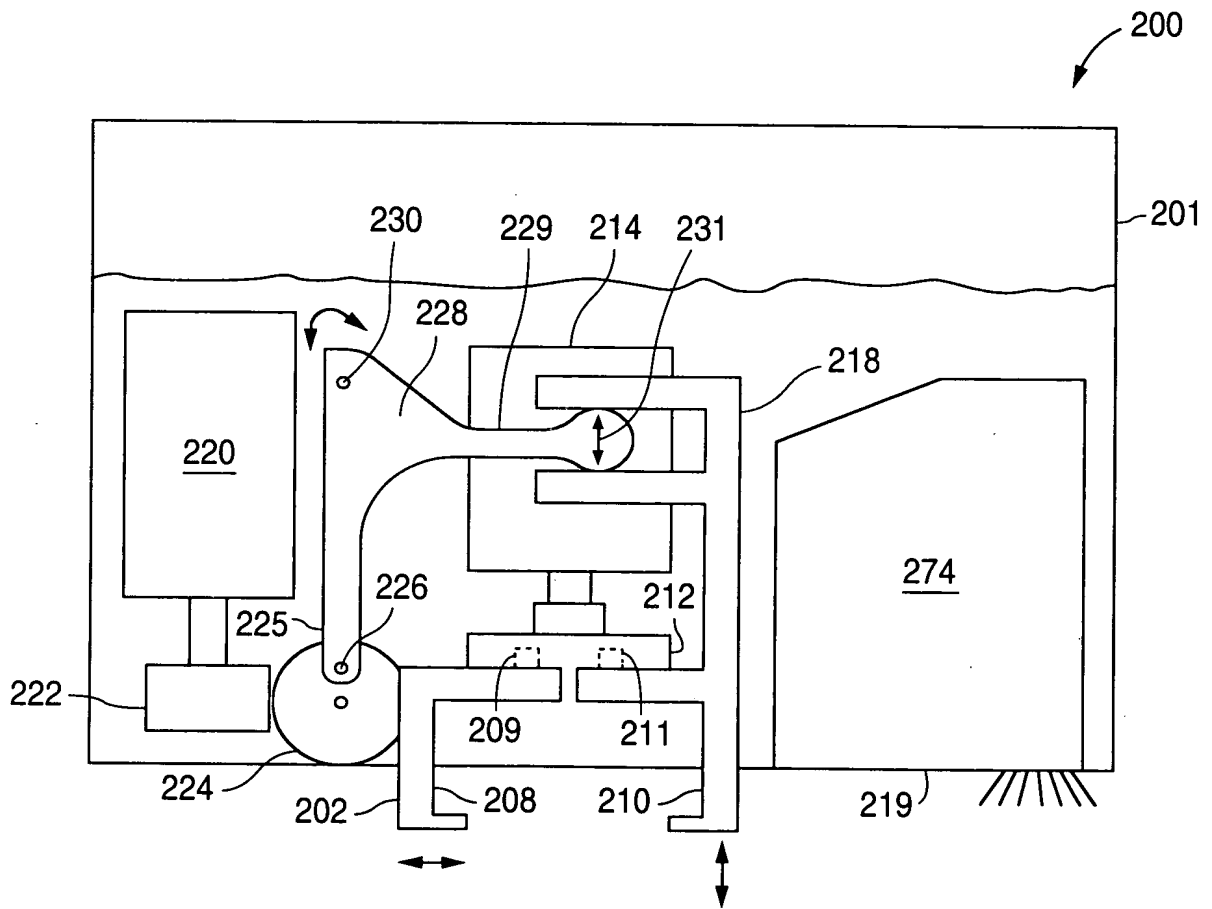
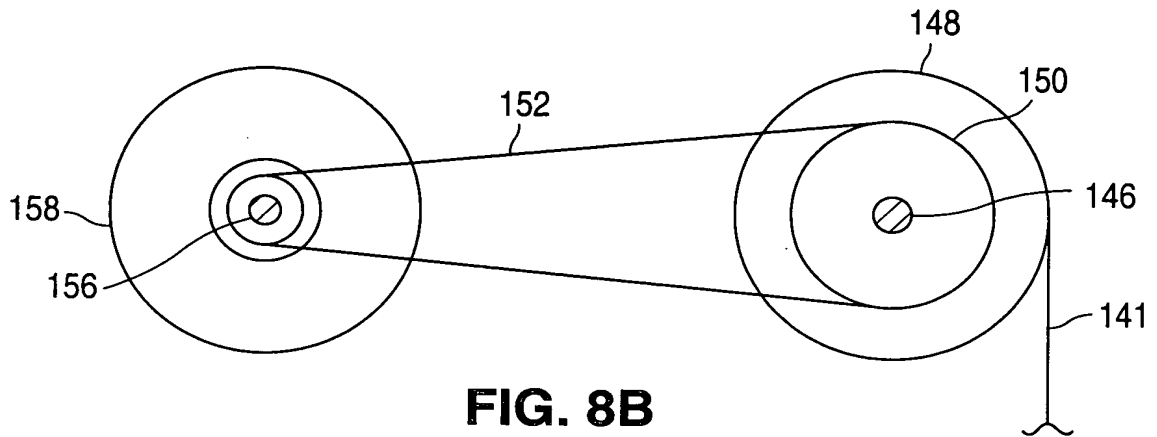


FIG. 9

A cross-sectional view of a semiconductor device 200. The device includes a substrate 72 with a central region containing a hatched area. A layer 201 is formed on the substrate. A dashed line 270 indicates an interface or boundary. A layer 252 is formed on top of the substrate, containing several rectangular features 256 and 258. A layer 254 is formed on top of the layer 252. A layer 260 is formed on top of the layer 254. A layer 262 is formed on top of the layer 260. A layer 270 is formed on top of the layer 262. A layer 250 is formed on top of the layer 270. A layer 258 is formed on top of the layer 250. A layer 262 is formed on top of the layer 258. A layer 270 is formed on top of the layer 262. A layer 252 is formed on top of the layer 270. A layer 254 is formed on top of the layer 252. A layer 260 is formed on top of the layer 254. A layer 262 is formed on top of the layer 260. A layer 270 is formed on top of the layer 262. A layer 250 is formed on top of the layer 270. A layer 258 is formed on top of the layer 250. A layer 262 is formed on top of the layer 258. A layer 270 is formed on top of the layer 262. A layer 252 is formed on top of the layer 270.

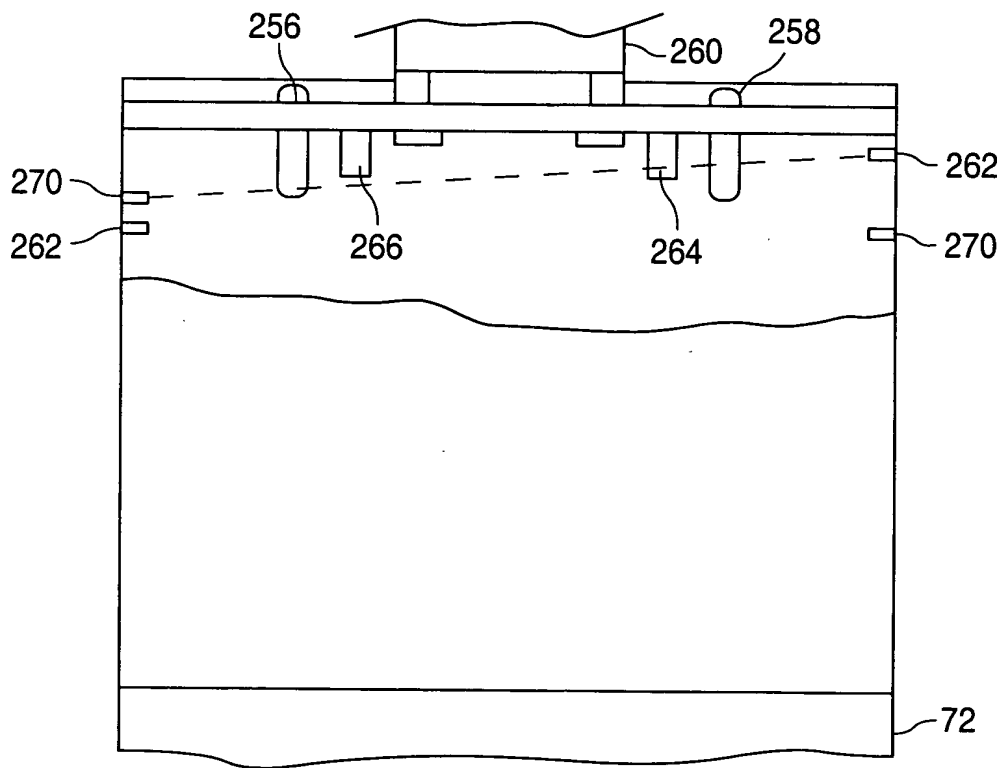


FIG. 12B

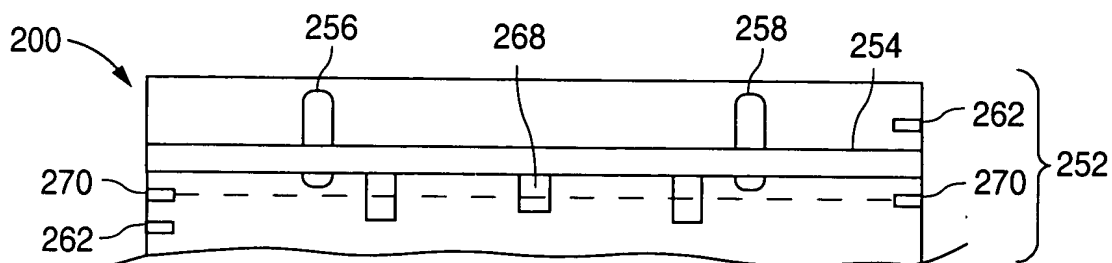


FIG. 12C

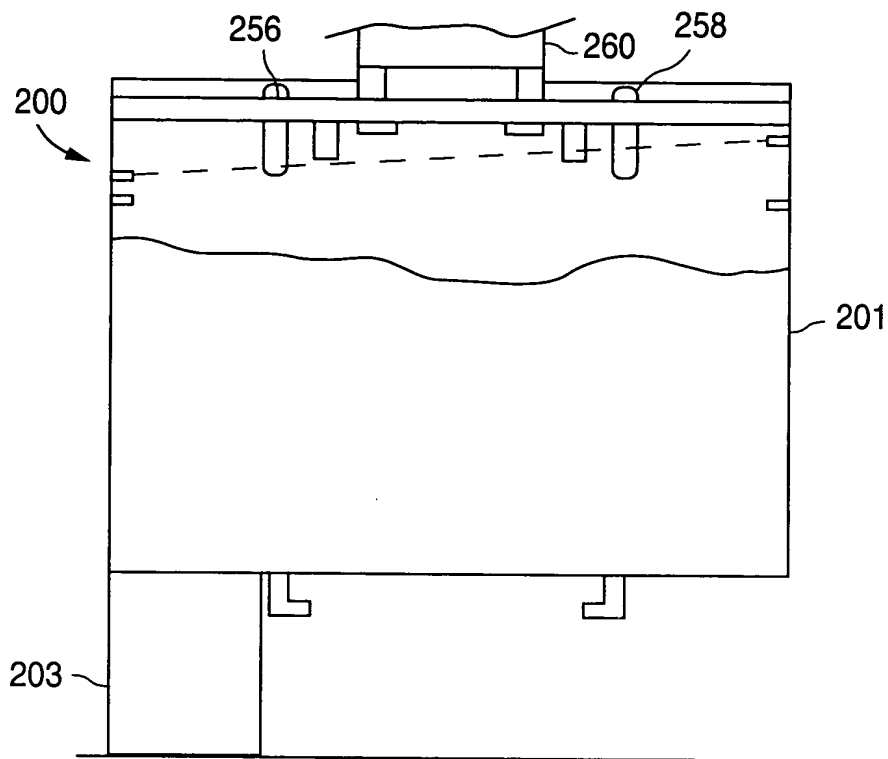


FIG. 12D

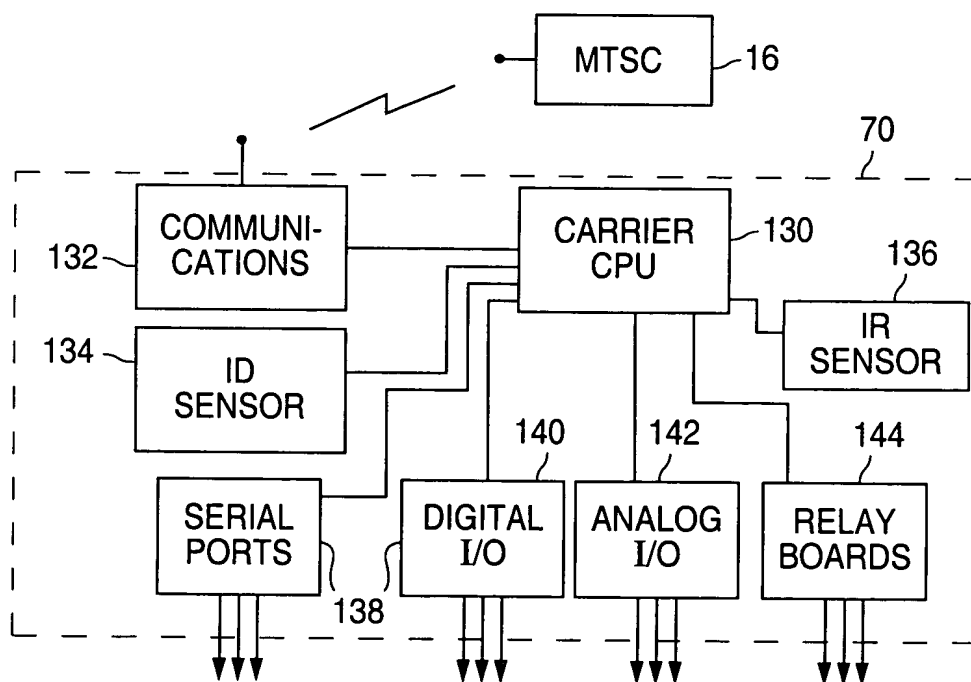


FIG. 13

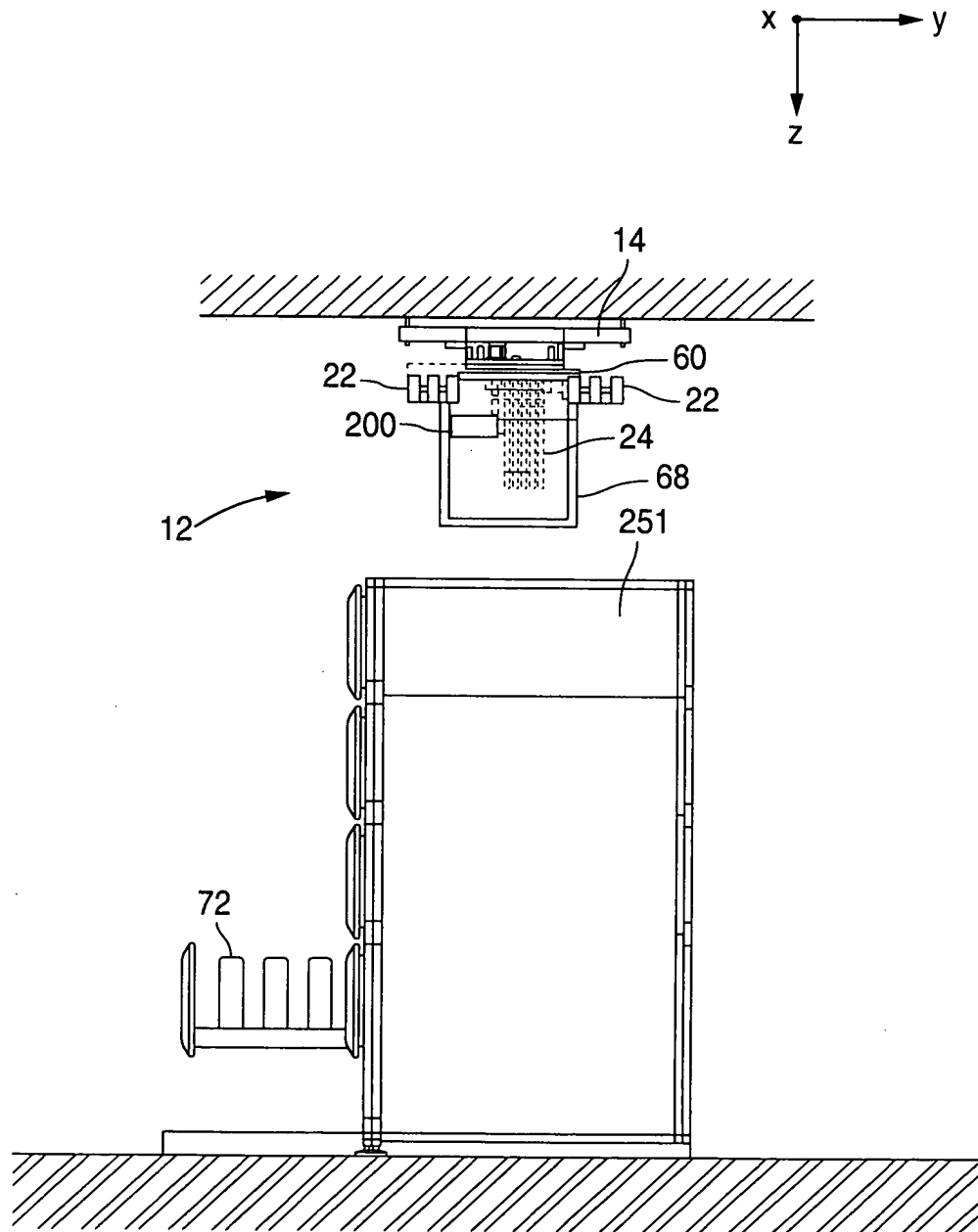


FIG. 14A

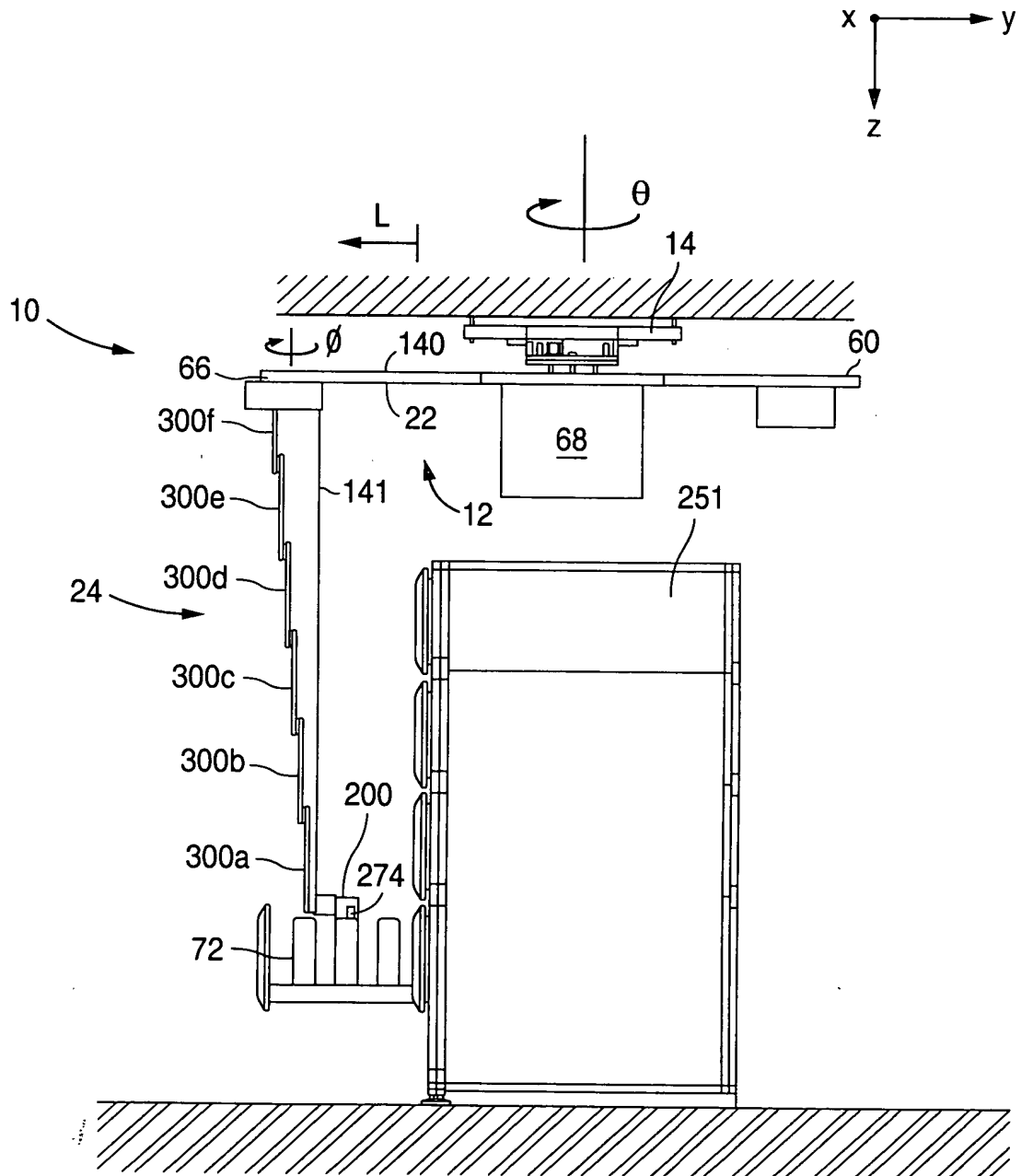


FIG. 14B

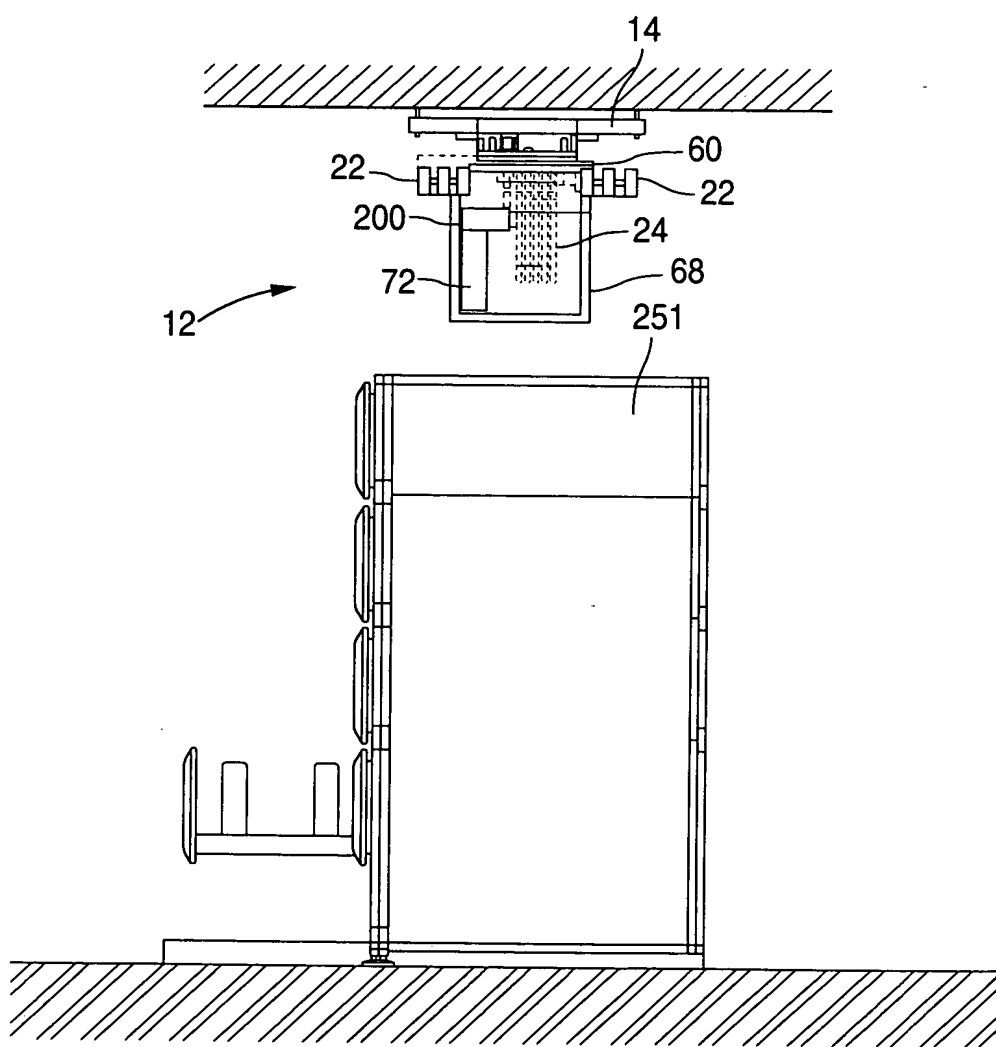
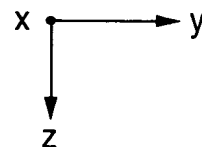


FIG. 14C

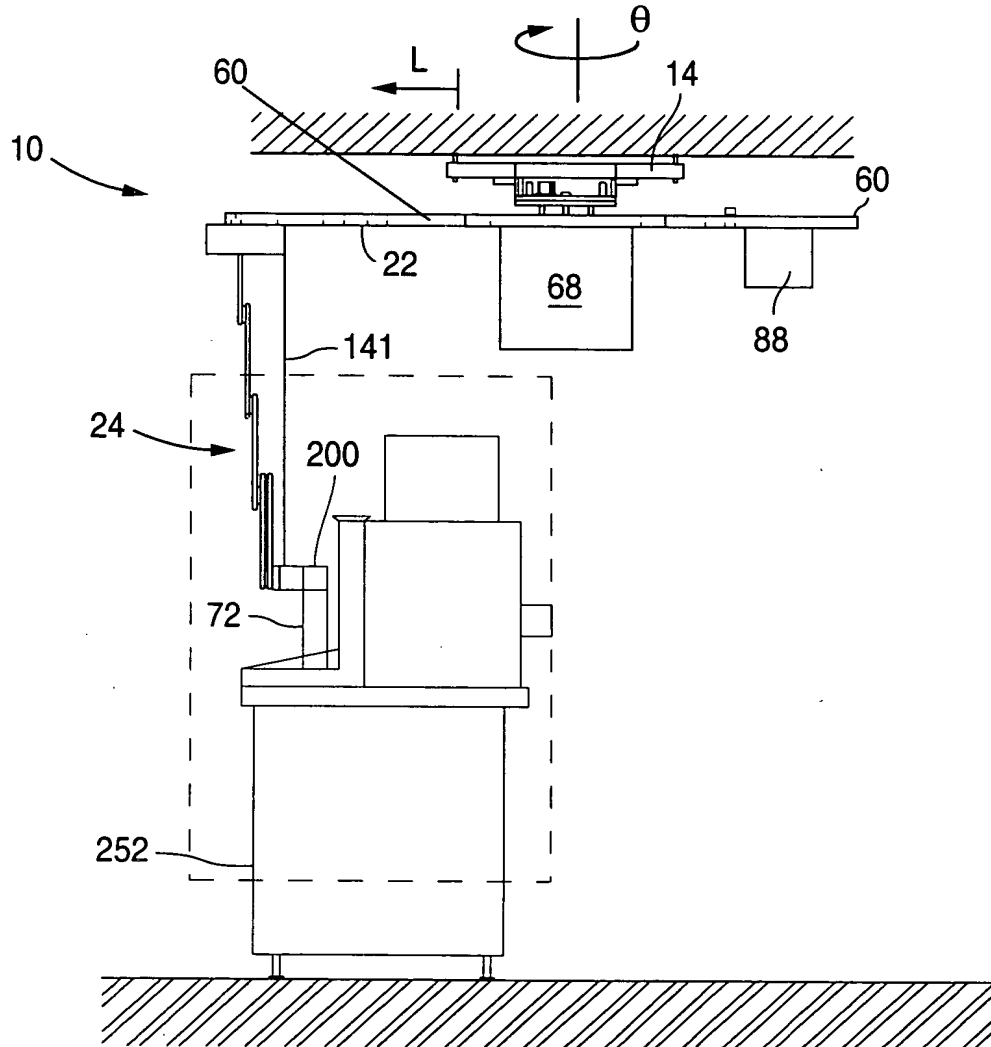


FIG. 14D

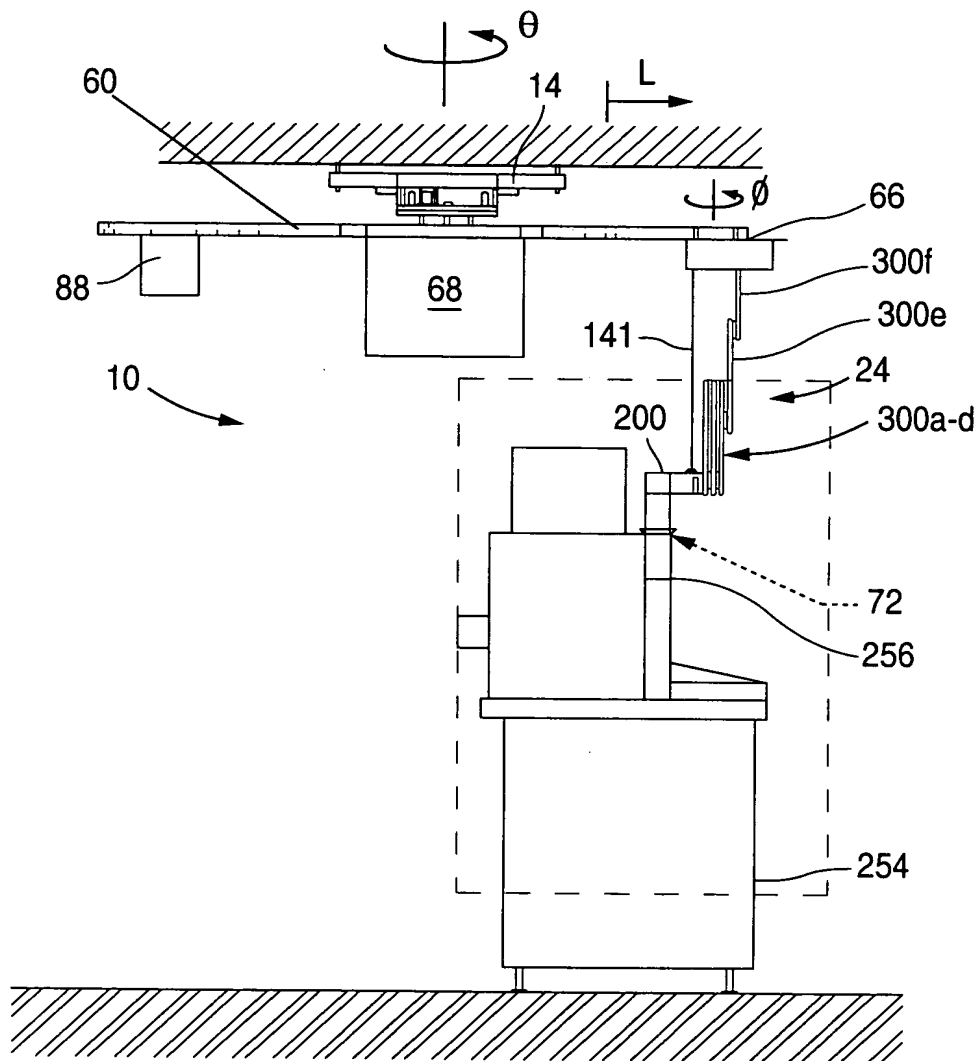


FIG. 14E